# Analysis of Adiabatic flip-flops for Ultra Low Power Applications

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# Abstract:

In this paper we have presented adiabatic flip flops which are used for clocking in digital systems. The clocking scheme using energy recovery technique has already appeared as a successful and promising scheme for limiting power dissipation in ultra low power digital systems. Adiabatic flip flops are the key elements for this type of energy efficient adiabatic clocking scheme. The flip-flops are working in adiabatic principle. Here in this work we have done the simulation and analyze the performance of two basic types of energy recovery flip flops. These are single ended conditional capturing flip-flop and differential conditional capturing flip flop. Both the flip-flops are utilizing energy recovery scheme. For better comparison results we have also used clock gating scheme along with energy recovery technique. Using cadence 180nm technology the simulations are obtained.

**Tools used:**

**Tanner**